In re Application of:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

James B. Johnson et al.

Serial No.: 09/809,608

Filed: March 15, 2001

Method and Apparatus for For:

> Compensating Duty Cycle Distortion in a Data Output Signal From a Memory

Device by Delaying and Distorting a

Reference Clock

88888888 Group Art Unit: 2116

Examiner:

Trujillo, James K.

Atty. Docket: MICS: 0070/FLE

(00-0917)

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November 19, 2004 Date

Christina Hartline

Sir:

TRANSMITTAL OF FORMAL DRAWINGS

Enclosed are six (6) sheets of formal drawings for the above-referenced patent application, which are attached as Appendix A.

Respectfully submitted,

Date: November 19, 2004

Brent R. Knight

Reg. No. 54,226 FLETCHER YODER

P.O. Box 692289

Houston, TX 77269-2289

(281) 970-4545